

What is claimed is:

1 1. A random access memory device in an integrated circuit chip, comprising:
2 a memory array of memory cells organized into rows and columns, including a
3 plurality of word lines and bit lines, each row of memory cells being coupled to a word line
4 and each column of memory cells being coupled to a bit line;
5 sense amplifier circuitry coupled to the bit lines and being selectively disabled;
6 address decode circuitry for receiving an address value and asserting a row line
7 associated therewith; and ✓
8 test circuitry, coupled to at least one bit line, for placing on an external pad of the
9 integrated circuit chip a current level corresponding to a voltage level appearing on the at
10 least one bit line, while concurrently disabling the sense amplifier circuitry.

1 2. The random access memory device of claim 1, wherein the random access ✓
2 memory device comprises a ferroelectric memory device.

1 3. The random access memory device of claim 1, wherein the random access ✓
2 memory device comprises a nonvolatile memory device.

1 4. The random access memory device of claim 1, wherein the sense amplifier
2 selectively drives the bit lines towards high and low reference voltage levels during normal
3 memory access operations, the random access memory device is selectively configured in ✓
4 a test mode of operation by the test circuitry, and the sense amplifier circuitry is disabled
5 from driving the bit lines by the test circuitry when the random access memory device is
6 in the test mode of operation.

1 5. The random access memory device of claim 4, wherein the random access
2 memory device includes a test input signal and is selectively configured in the test mode
3 of operation based upon a value of the test input signal.

1 6. The random access memory device of claim 1, wherein the external pad is sized
2 to contact and electrically connect to (a tester probe) and the test circuitry comprises a pair ?
3 of series-connected transistors coupled between the external pad and a reference voltage
4 level, the pair of series-connected transistors including a first transistor having a control
5 terminal coupled to the at least one bit line.

1 7. The random access memory device of claim 6, wherein the pair of series-
2 connected transistors further comprises a second transistor having a control terminal ✓
3 connected to a control signal that selectively activates the second transistor.

1 8. The random access memory device of claim 1, wherein the external pad is sized
2 to contact and electrically connect to (a tester probe) and the test circuitry comprises a
3 plurality of pairs of series-connected transistors coupled between the pad and a reference
4 voltage level, each pair of series-connected transistors including a first transistor having
5 a control terminal coupled to (distinct bit line.)

1 9. The random access memory device of claim 8, wherein each pair of series-
2 connected transistors comprises a second transistor having a control terminal connected to ✓
3 a control signal that selectively activates the second transistor.

1 10. The random access memory device of claim 9, further comprising a selection
2 circuit that selectively activates the second transistors of the plurality of pairs of series- ✓
3 connected transistors in a sequential manner.

1 11. The random access memory device of claim 10, wherein the selection circuit
2 comprises counter circuitry and decode circuitry having a plurality of output signals such
3 that each output signal is connected to the control terminal of (a distinct second transistor)

1 12. The random access memory device of claim 1, wherein the test circuitry
2 comprises:

3 a first pair of series-connected transistors connected between the external pad of the
4 integrated circuit chip and a reference voltage level, a first transistor of the first pair of
5 series-connected transistors having a control terminal connected to the at least one bit line;
6 and

7 a second pair of series-connected transistors connected between (a second pad) of the
8 integrated circuit chip and the reference voltage level, a first transistor of the second pair
9 of series-connected transistors having a control terminal connected to (a third pad) of the
10 integrated circuit chip and a second transistor of the second pair of series-connected
11 transistors being activated.

1 13. The random access memory device of claim 1, further comprising:

2 calibration test circuitry for providing (a relationship) between the current level } ?
3 placed on the external pad and the voltage level appearing at the at least one bit line. }

1 14. The random access memory device of claim 13, wherein the calibration test
2 circuitry has substantially (the same structure as a portion of the test circuitry.)

1 15. The random access memory device of claim 13, wherein the calibration test
2 circuitry comprises:

3 an input connected to (a second external pad) for externally controlling the operating
4 characteristics of the calibration circuit; and

5 an output connected to (a third external pad) for externally measuring a current
6 flowing through the calibration test circuitry.

1 16. A method of testing a semiconductor memory device having an array of
2 memory cells and sense amplifier circuitry coupled to bit lines of the array, the
3 semiconductor memory device being in an integrated circuit chip, the method comprising:

4 connecting memory cells in a row of memory cells to bit lines of the array;

5 disabling the sense amplifier circuitry from driving the bit lines;

6 selecting a bit line; and

7 providing a current level to a pad in the integrated circuit chip corresponding to a
8 voltage level appearing on the selected bit line.

1 17. The method of claim 16, wherein:

2 the semiconductor memory device comprises a ferroelectric memory device. ✓

1 18. The method of claim 16, further comprising measuring the current level ✓
2 provided to the pad.

1 19. The method of claim 16, further comprising:

2 repeating the steps of selecting and providing, with each step of selecting —
3 comprising selecting a different bit line in the array.

1 20. The method of claim 16, further comprising the step of:

2 determining a relationship between the current level provided to the pad and the
3 voltage level appearing on the selected bit line; and
4 mapping the current level provided to a voltage level appearing across a memory
5 cell connected to the selected bit line. 0

1 21. The method of claim 16, further comprising the steps of:

2 disconnecting the row of memory cells from the bit lines; ✓

3 connecting another row of memory cells to the bit lines; and ✓
4 repeating the steps of selecting and providing for the another row of memory cells.

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1 22. An apparatus, comprising:
2 a random access memory device, comprising:
3 a memory array of memory cells organized into rows and columns, including a
4 plurality of word lines and bit lines, each row of memory cells being coupled to a word line
5 and each column of memory cells being coupled to a bit line;
6 address decode circuitry for receiving an address value and asserting a row line ✓
7 associated therewith; and
8 test circuitry, coupled to at least one bit line for placing on an external pad a current
9 level corresponding to a voltage level appearing on the at least one bit line.

1 23. The apparatus of claim 22, wherein the random access memory device
2 comprises a ferroelectric memory device. ✓

1 24. The apparatus of claim 22, wherein the random access memory device ✓
2 comprises a nonvolatile memory device.

1 25. The apparatus of claim 22, wherein the random access memory device
2 comprises sense amplifier circuitry that selectively drives the bit lines towards high and low
3 reference voltage levels during normal memory access operations, the random access
4 memory device is selectively configured in a test mode of operation by the test circuitry and
5 the sense amplifier circuitry is disabled from driving the bit lines by the test circuitry when
6 the random access memory device is in the test mode of operation.

1 26. The apparatus of claim 22, wherein the apparatus further comprises:
2 a processing unit having an address port connected to an address input port of the
3 random access memory device and a data port connected to a data port of the random
4 access memory device.

1 27. The apparatus of claim 22, wherein the external pad is sized to receive a tester
2 probe) and the test circuitry comprises a pair of series-connected transistors coupled
3 between the external pad and a reference voltage level, the pair of series-connected
4 transistors including a first transistor having a control terminal coupled to the at least one
5 bit line.

1 28. The apparatus of claim 27, wherein the pair of series-connected transistors
2 further comprises a second transistor having a control terminal connected to a control
3 signal that selectively activates the second transistor. ✓

1 29. The apparatus of claim 22, wherein the external pad is sized to receive a tester
2 probe, and the test circuitry comprises a plurality of pairs of series-connected transistors
3 coupled between the external pad and a reference voltage level, each pair of series-
4 connected transistors including a first transistor having a control terminal coupled to
5 (distinct bit line.) ✓

1 30. The apparatus of claim 29, wherein each pair of series-connected transistors
2 comprises a second transistor having a control terminal connected to a control signal that
3 selectively activates the second transistor. ✓

1 31. The apparatus of claim 30, wherein the test circuitry comprises a selection
2 circuit that selectively activates the second transistors of the plurality of pairs of series-
3 connected transistors in a sequential manner. ✓

1 32. The apparatus of claim 31, wherein the selection circuit comprises counter
2 circuitry and decode circuitry having (a distinct output signal) connected to the control
3 terminal of each of the second transistors.

1 33. The apparatus of claim 22, wherein the test circuitry comprises:
2 a first pair of series-connected transistors connected between the external pad of the
3 apparatus and a reference voltage level, a first transistor of the first pair of series-connected
4 transistors having a control terminal connected to the at least one bit line; and
5 a second pair of series-connected transistors connected between (a second pad) of the
6 apparatus and the reference voltage level, a first transistor of the second pair of series-
7 connected transistors having a control terminal connected to (a third pad) of the apparatus
8 and (a second transistor of the second pair of series-connected transistors being activated.)

1 34. The apparatus of claim 22, wherein the random access memory device further
2 comprises:
3 calibration test circuitry for providing (a relationship between the current level and
4 the voltage level) appearing at the at least one bit line.

1 35. The apparatus of claim 34, wherein the calibration test circuitry has
2 substantially the same structure as a portion of the test circuitry. 10

1 36. The apparatus of claim 34, wherein the calibration test circuitry comprises:
2 an input connected to a second external pad for externally controlling the operating
3 characteristics of the calibration circuit; and
4 an output connected to a third external pad for externally measuring a current
5 flowing through the calibration test circuitry. 10

1 37. An apparatus, comprising:
2 a ferroelectric capacitor; and
3 means for placing on an external pad of the apparatus a current level corresponding
4 to a voltage level appearing across the ferroelectric capacitor. ✓

1 38. The apparatus of claim 37, wherein the means for placing comprises a first
2 transistor having a control terminal coupled to a plate of the ferroelectric capacitor, a first
3 conduction terminal coupled to the external pad and a second conduction terminal coupled
4 to a voltage reference. ✓

1 39. The apparatus of claim 38, wherein the means for placing further comprises a
2 second transistor series connected to the first transistor to form a pair of series connected
3 transistors connected between the external pad and the voltage reference, and a means for
4 selectively activating the second transistor.

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